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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/866,656	05/30/2001	Sung-Il Park	8733.434.00	5149

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EXAMINER
QI, ZHI QIANG

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 11/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/866,656	PARK ET AL.	
	Examiner	Art Unit	
	Mike Qi	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2004 and 18 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22 and 24* is/are rejected.

7)☐ Claim(s) *23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on Sep. 27, 2004 has been entered.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant admitted prior art (AAPA) in view of US 6,621,517 (Kang).

Claims 1, 14 and 20, AAPA discloses (paragraph 0002 – 0028; Figs.1-6) that generally, a liquid crystal display device having a liquid crystal panel comprising:

- a first (lower) substrate (20), a second (upper) substrate (10), the first (lower) substrate (20) having a plurality of source pads (30 of Figs.3 - 4) and gate pads (28 of Figs.3 - 4) (because the FPC 40 as the gate transmitting lines formed on the lower substrate 20), and the first (lower) and second (upper) substrates (20, 10) being attached;

- a first printed circuit board (source PCB 33) connected to the plurality of source pads (30 of Fig.4), and the source PCB (33) applying signals to the source pads (30 of Fig.4);
- a second printed circuit board (gate PCB 31) connected to the plurality of gate pads (28 of Fig.4), and the gate PCB (31) applying signals to the gate pads (28 of Fig.4);
- a plurality of gate transmitting lines (FPC 40 transmits the gate signals) formed directly on the lower substrate (20) and connecting the gate pads (28 of Fig.4) with the source pads (30 of Fig.4), the plurality of gate transmitting lines (FPC 40) transmitting signals from the source PCB (33) to the gate PCB (31) via the gate transmitting lines (FPC 37 or 40).

AAPA does not explicitly disclose that a first gate transmitting line of the plurality of gate transmitting lines has a first resistance, and the plurality of gate transmitting lines other than the first gate transmitting line have a second resistance, and the first resistance is less than the second resistance or one of the gate lines has a first resistance and the other gate lines have a second resistance greater than the first resistance.

However, Kang discloses (col.12, lines 45-52; Fig.6) that the value of the resistance from the first gate line (353e) to the last gate line (353j) of a plurality of gate lines connected to a gate-driving IC (332d) is increased, so that the resistance applied to the first gate line (353e) is the smallest, such that the resistance applied to the other gate lines is greater than the first resistance, i.e., a first gate line has a first resistance

and the other plurality of gate lines have a second resistance and the first resistance is less than the second resistance. Kang indicates (col.2, lines 2-18) that in order to prevent imbalance in brightness of a liquid crystal display device due to a delay and a distortion of a gate-driving signal by adjusting a signal level of a gate-driving signal delayed and modulated. So that by adjusting the resistance of the gate lines as the first gate line has a smallest resistance and the other gate lines have a greater resistance would prevent the imbalance in brightness of a liquid crystal display device.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to arrange the first gate line has a smallest resistance and the other gate lines have a greater resistance as claimed in claims 1, 14 and 20 for preventing the imbalance in brightness of a liquid crystal display device.

Claims 2 and 15, AAPA discloses (paragraph 0015-0019; Figs.3 - 4) that the plurality of gate transmitting lines (40) include at least eight signal lines for transmitting signals from the source PCB (33) to the gate PCB (31).

Claims 3-9 and 16-17, AAPA discloses (paragraph 0015-0019; Figs.3-4) that the gate transmitting lines (FPC 37 or 40 transmits the gate signals) include Vcom (common voltage signal line); Vgh (gate high voltage signal line); Vgl (gate low voltage signal line); Gsc and Goe (to control the signal passing through the gate line); Gsp (to control the drive IC); Vcc (power line) and Vdd (ground line).

Claims 10-12 and 18-19, AAPA discloses (paragraph 0023) that dummy pads are preferably formed in gaps between adjacent gate pads (28) and between adjacent

source pads (30), so as to prevent an abnormal electrical interaction between the adjacent gate transmitting wires, and that would have been at least obvious.

Claim 13, AAPA discloses (paragraph 0020; Fig.3) that a plurality of connecting wires (i.e., the FPC 40 transmitting gate signals as the gate transmitting lines) are formed directly on the lower substrate (20).

Claim 24, AAPA discloses (paragraph 0020; Fig.3) that the gate transmitting lines (FPC 40) transmits the gate signals, inherently, one of the gate transmitting lines transmits a gate voltage signal (the lowest voltage must be transmitted by the first transmitting line), and that must include a gate low voltage scanning signal.

3. Claims 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Kang as applied to claims 1-20 and 24 above, and further in view of US 5,748,179 (Ito et al).

Claims 21-22, lacking limitation is such that the first resistance of the first gate transmitting line is below 30 Ω.

However, Ito discloses (col.7, line 56 – col.8, line 13; Fig.5) that the resistance value from the connection portion of the input wire (Td) with the flexible board to the input terminal (IP) is equal to several ohms. Further, the input terminal portion itself is required to have a resistance value of several ohms. Therefore, the signal transmitting lines in LCD are required to have a resistance value of several ohms that is below 30 Ω.

Ito indicates (col.16, lines 17 – 34) that larger resistance occurs at the gate side, and at the drain side would cause a distortion amount of the output waveform of the driving IC is varied every wiring, and this finally causes unevenness of a display

image. Therefore, it is necessary to reduce the resistance of the signal transmitting lines in order to reduce the signal distortion and prevent the unevenness of a display image.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to arrange the first gate line having a resistance below 30 Ω as claimed in claims 21-22 for reducing the signal distortion and preventing the unevenness of a display image.

Allowable Subject Matter

4. Claim 23 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record neither discloses nor teaches a liquid crystal display panel comprising various elements as claimed, more specifically, as the following:

The gate transmitting lines having a first resistance value for the first gate transmitting line and a second resistance value for the other gate transmitting lines, and the first resistance value is less than the second resistance value which is about 100 Ω [claim 23].

The closest references Kang and Ito disclose that the gate transmitting lines having different resistances such as several ohms, but none of the prior art of record teaches that the second resistance value is about 100 Ω as claimed in claim 23.

Response to Arguments

5. Applicant's arguments filed Sep.17, 2003 have been fully considered but they are not persuasive.

Applicant's arguments are as follows:

1) None of the references teach or suggest a set of gate transmitting line having different resistances, such that the signals are transmitted without distortion as claimed in claims 1, 14 and 20.

Examiner's responses to Applicant's arguments are as follows:

1) The reference Kang discloses (col.12, lines 45-52; Fig.6) that the value of the resistance from the first gate line (353e) to the last gate line (353j) of a plurality of gate lines connected to a gate-driving IC (332d) is increased, so that the resistance applied to the first gate line (353e) is the smallest, such that the resistance applied to the other gate lines is greater than the first resistance, i.e., a first gate line has a first resistance and the other plurality of gate lines have a second resistance and the first resistance is less than the second resistance. Kang indicates (col.2, lines 2-18) that in order to prevent imbalance in brightness of a liquid crystal display device due to a delay and a distortion of a gate-driving signal by adjusting a signal level of a gate-driving signal delayed and modulated. So that by adjusting the resistance of the gate lines as the first gate line has a smallest resistance and the other gate lines have a greater resistance would prevent the imbalance in brightness of a liquid crystal display device.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1) US 6,639,589 B1 (Kim et al) discloses (col.8, lines 28-53, Figs. 2-6) that in order to prevent the gate driving signal transmission delay, the resistance between the transmission pattern and the transmission lines needs to be decreased that is the first gate line having a larger resistance than the other gate lines. Such that is the gate transmitting lines having different resistance, and one of the plurality of gate transmitting lines having a first resistance and the others of the plurality of gate transmitting lines having a second resistance as long as the resistance are different so as to prevent the gate driving signal transmission delay.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (571) 272-2299. The examiner can normally be reached on M-T 8:00 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mike Qi
November 1, 2004

TARIFUR R. CHOWDHURY
PRIMARY EXAMINER